

FIG.2 PRIOR ART

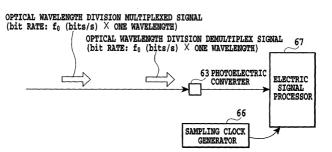


FIG.3
PRIOR ART

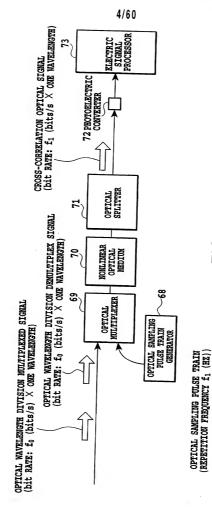


FIG.4 Prior art

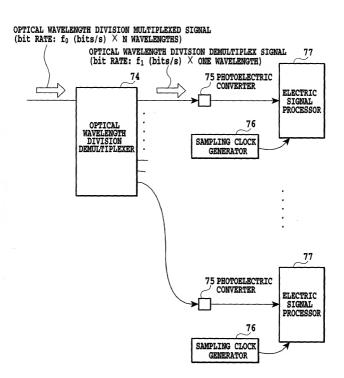


FIG.5
PRIOR ART

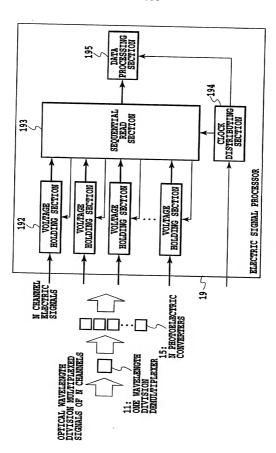


FIG.7

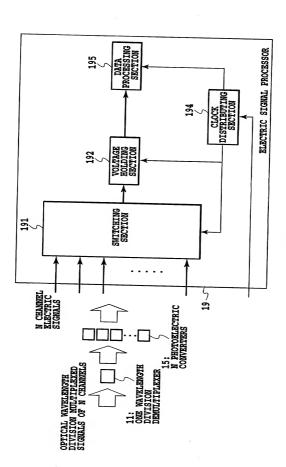


FIG.8

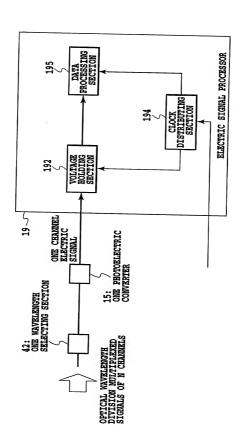


FIG.9

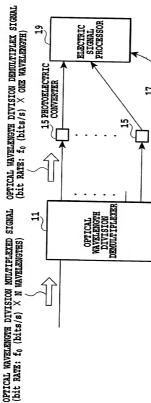
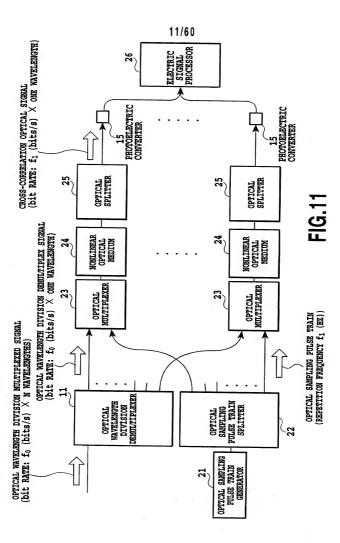


FIG.10

SAMPLING CLOCK GENERATOR



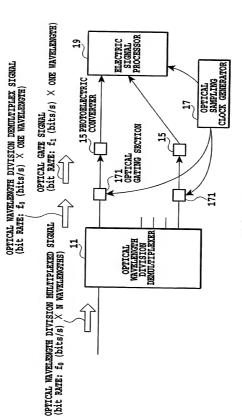


FIG.12

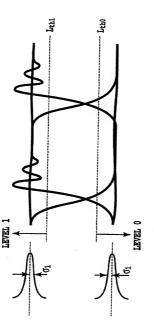


FIG.13

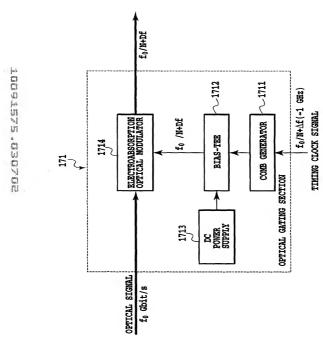


FIG.14

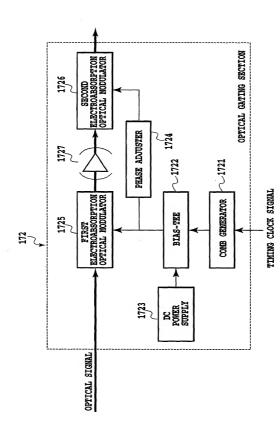


FIG.15

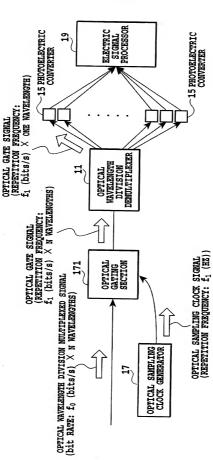


FIG.16

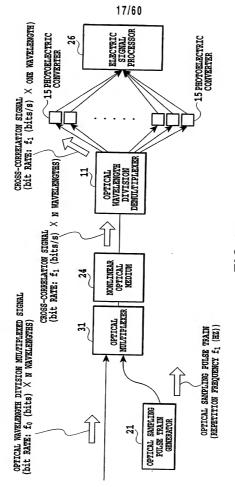


FIG.17

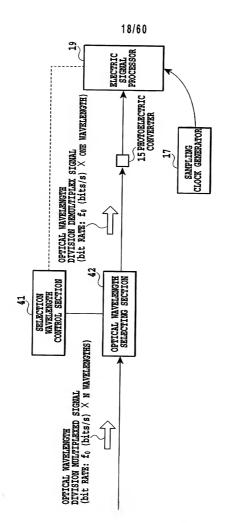


FIG. 18

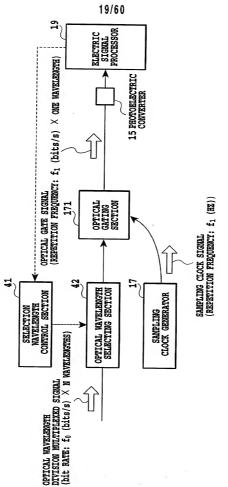


FIG.19

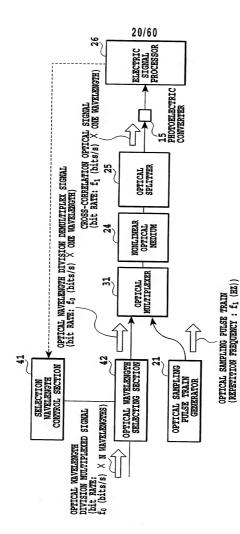


FIG.20

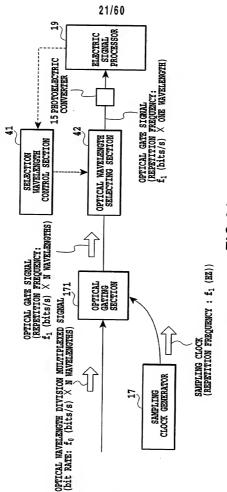


FIG.21

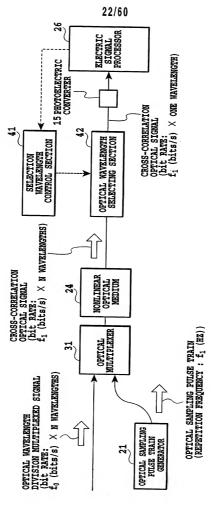


FIG.22

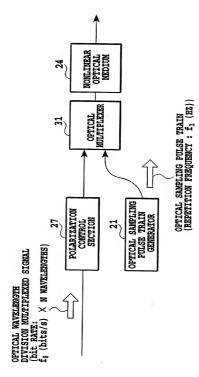


FIG.23

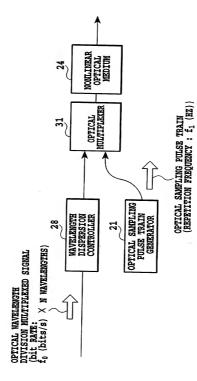


FIG.2/

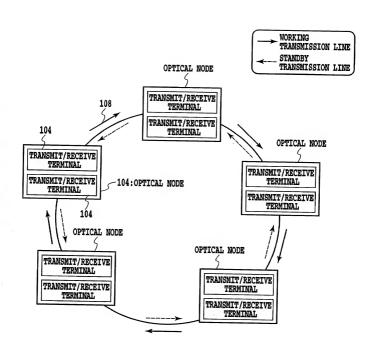


FIG.25A

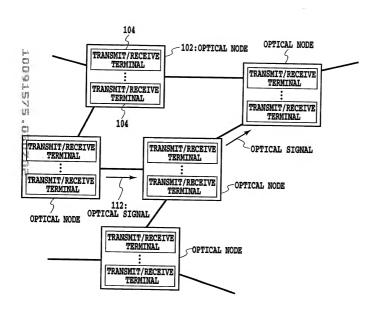


FIG.25B



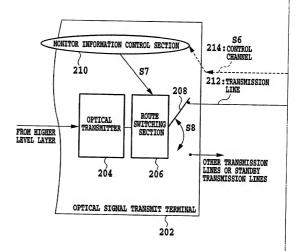


FIG.26A

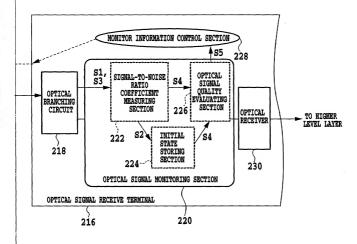


FIG.26B

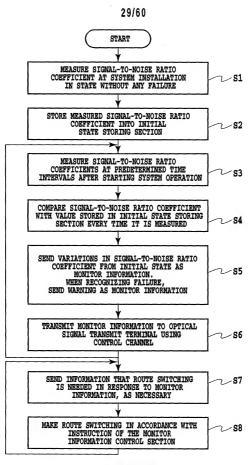


FIG.27

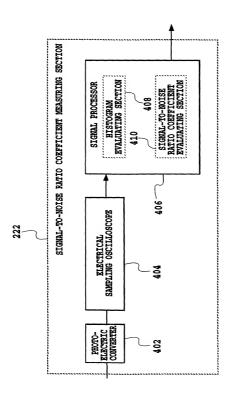


FIG.28

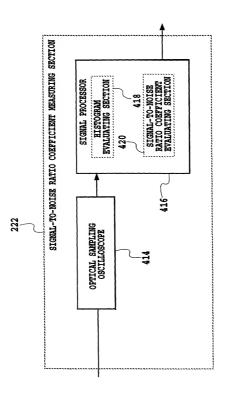


FIG.29

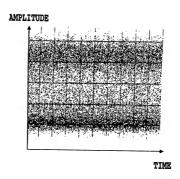


FIG.30A

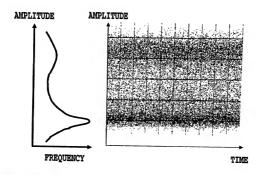


FIG.30B

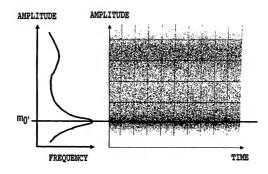


FIG.31A

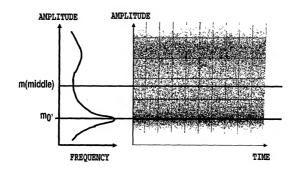


FIG.31B

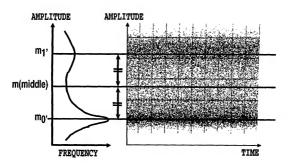


FIG.32A

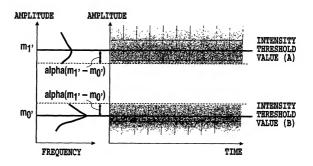


FIG.32B

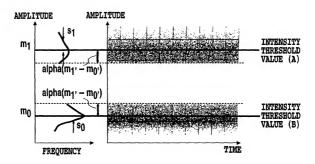


FIG.33A

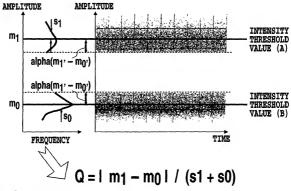


FIG.33B

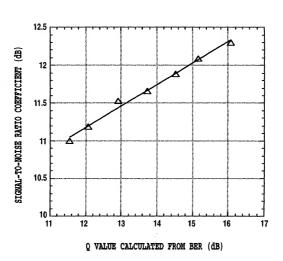


FIG.34

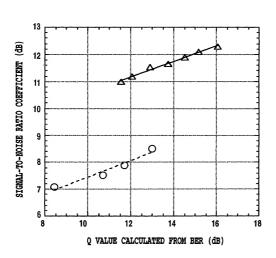


FIG.35

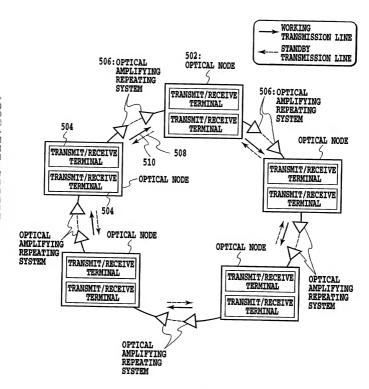


FIG.36A

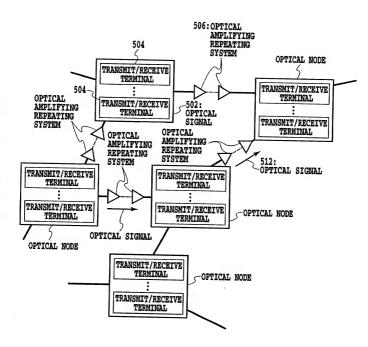
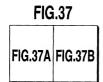


FIG.36B



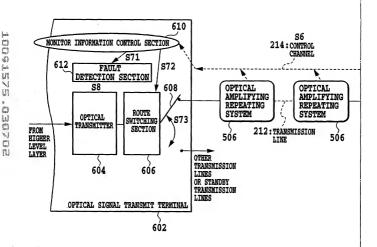


FIG.37A

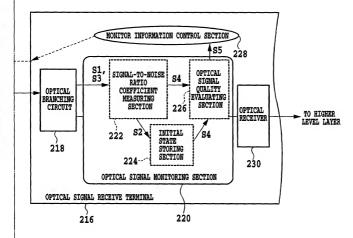


FIG.37B

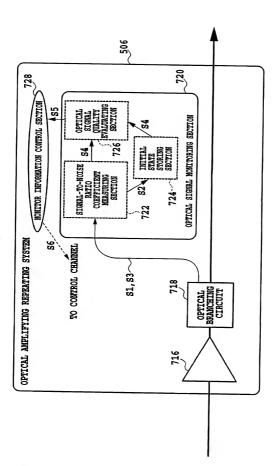


FIG.38

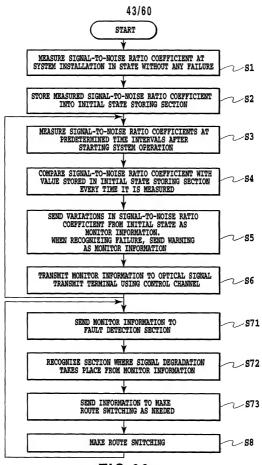


FIG.39

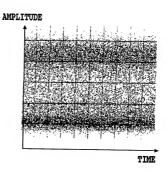


FIG.40A

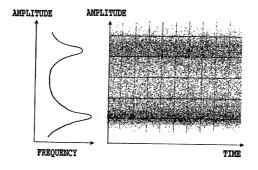


FIG.40B

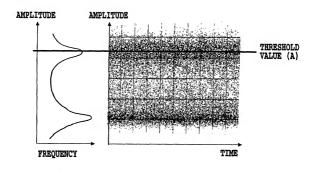


FIG.41A

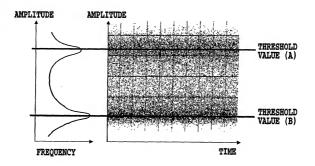


FIG.41B

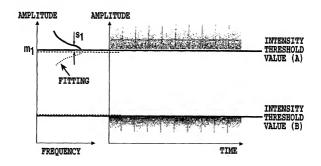


FIG.42A

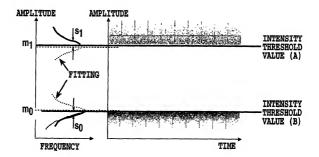


FIG.42B

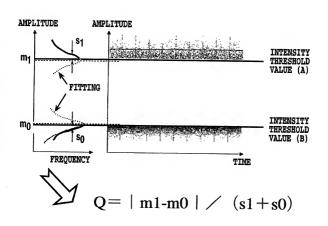


FIG.43

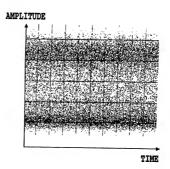


FIG.44A

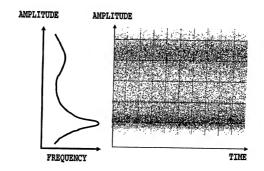


FIG.44B

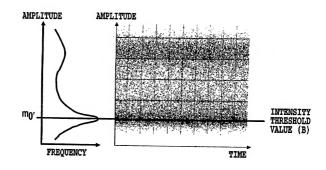


FIG.45A

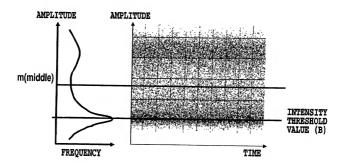


FIG.45B

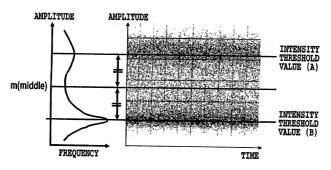


FIG.46A

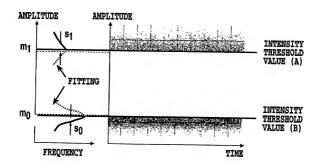


FIG.46B

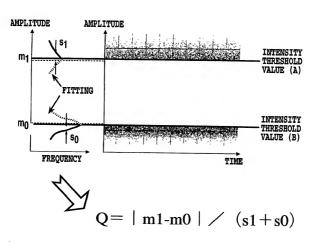


FIG.47

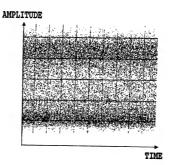


FIG.48A

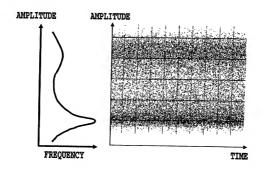


FIG.48B

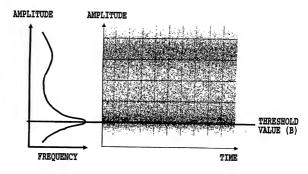


FIG.49A

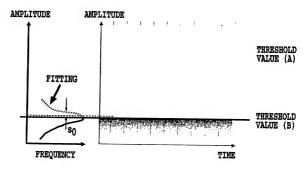


FIG.49B

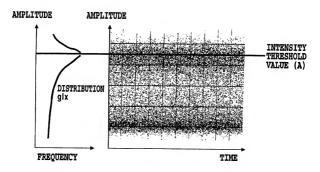


FIG.50A

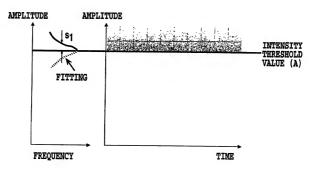


FIG.50B

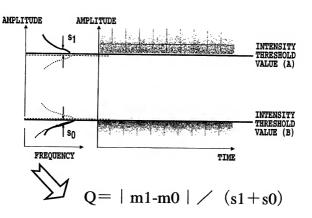


FIG.51

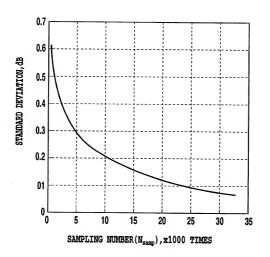


FIG.52

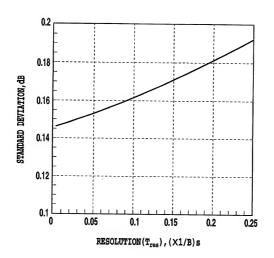


FIG.53A

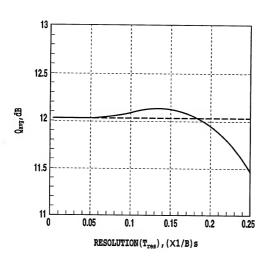


FIG.53B

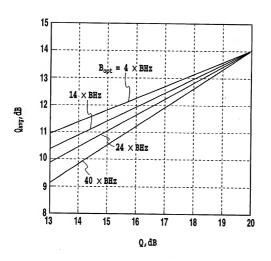


FIG.54A

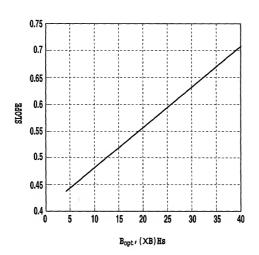


FIG.54B